UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/784,274	02/13/2001	Mark Peting	004559P019	3064

7590 02/13/2004

Thomas C Webster
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025

EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	10

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/784,274	PETING ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to amendment filed 12/2/2003 (paper no. 9).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,453,370 hereinafter Stracovsky) in view of Katayama et al. (US PAT. 5,875,452 hereinafter Katayama).

Regarding claim 1, Stracovsky discloses a method comprising detecting a write data burst (col. 27 lines 5-23), determining if at least one memory unit is available to receive the write data burst (col. 12 lines 29-56), writing the write data burst to the at least one memory unit if the at least one memory unit is available to receive data (col. 9 lines 33-63 and col. 15 lines 4-8), concurrently with activating the at least one memory unit to receive data, if the at least one memory unit is not available to receive data, i.e., activating any of the available memory bank based on the result of comparison between the status stores in the tag register and the requested command (col. 11 line 29 through col. 12 line 24 and col. 20 lines 26-45) and further corresponding to each data burst (col. . 21 line 51 through col. 22 line 28). Stracovsky differs from the claimed invention in not specifically teaches storing a first portion of the write data burst in a buffer, and writing a second portion of the write data burst to the at least one memory unit when the at least one memory unit is available to receive data, writing the first portion of the write data burst from the buffer to the at least one memory unit after writing the second portion of the write data burst. However Katayama teaches a method for controlling data reads and writes from and to a DRAM array and its refreshing comprising the steps of writing a first portion of write data burst in a buffer (52, figure 2) concurrently with activating at least one memory unit if the at least one memory unit is busy, writing a second portion to the at least one memory unit when the at least one memory unit is available to receive data and writing the first portion of the write data burst from the buffer to the at least one memory unit after writing the second portion of the write data burst (col. 21 line 1 through col. 23 line 67 and col. 24 line 66 through col. 25 line 16) in order to prevent data writes from waiting to the execution of refreshing regardless of the timing with which writes are carried out (col. 6 line 46 through col. 8

line 18 and). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the shared memory system of Stracovsky in storing a first portion of the write data burst in a buffer, and writing a second portion of the write data burst to the at least one memory unit when the at least one memory unit is available to receive data, writing the first portion of the write data burst from the buffer to the at least one memory unit after writing the second portion of the write data burst, as per teaching of the Katayama, because it prevents data writes from waiting to the execution of refreshing regardless of the timing with which writes are carried out, thereby a plurality of unit data can be read or written in a constant and short access time regardless of the timing which the read or write of the specified size of data is executed.

Regarding claim 2, the difference between Stracovsky and the claims is the claims specifically recite the write data burst comprises at least eight data words. However, having this sized data burst does not have a disclosed purpose nor is this size disclosed to overcome any deficiencies in the prior art. As such, the data burst may have been of any size. In addition, Stracovsky discloses the burst data transfer comprises four data streams (col. 27 lines 5-24), the ordinary artisan would realize a possible data burst capacity increase as the current technology would warrant. Accordingly, it would have been an obvious matter of design choice to utilize the system of Stracovsky wherein the write data burst comprises four data streams, as disclosed above, since applicant has not disclosed that at least eight data words, as opposed to other sizes, overcomes a deficiency in the prior art or is for any stated purpose.

Regarding claim 3, Stracovsky discloses the first portion write data burst comprise at least one data word (col. 13 lines 1-3).

Regarding claim 4, Stracovsky discloses the write data burst comprises a write data burst during a processor's burst write mode (col. 27 lines 5-23).

Regarding claim 5, Stracovsky discloses the method is used in shared bus architecture (col. 1 lines 32-35).

Regarding claim 6, Stracovsky differs from the claimed invention in not specifically teaches the first portion of the write data burst and the second portion of the write data burst are stored in contiguous memory locations. However, Katayama teaches to store the write data burst in contiguous memory location (col. 18 lines 57-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the shared memory system of Stracovsky in having the first portion of the write data burst and the second portion of the write data burst are stored in contiguous memory locations, as per teaching of Katayama, because it not only reduces the number of pin connections required to transfer a multi-word burst of data between a port and a shared memory, but also increase the a multi-word burst of data access which can complete in a single memory access cycle in order to reduce the latency and collision of the memory access.

Regarding claim 7, Stracovsky discloses the first portion of the write data burst and the second portion of the write data burst are stored in non-contiguous memory location, i.e., non-sequential access which based on the availability and status of each memory bank, and the memory controller further comprising a reordering circuitry to re-generate the order of access which related to the on the availability and status of each memory bank (col. 19 lines 11-62).

Regarding claim 8, Stracovsky discloses the at least one memory unit comprise a Synchronous Dynamic Random Access Memory (SDRAM) bank (col. 6 lines 40-42 and col. 29 lines 44-45).

Regarding claims 9, 17, 20, 24 and 28 the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claims 10, 18, 25 and 29 the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 11, 19, 22, 26 and 30 the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 12 and 21, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 13, 23 and 27, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 14, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 15, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claims 16 and 31, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Response to Arguments

4. Applicant's arguments with respect to claims 1-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Zeller et al. (US PAT. 5,761,725) discloses a cache based computer system with cache write back suppression and processor peripheral communication suppression for data coherency (abstract).

Kasebayashi et al. (US PAT. 5,758,191) discloses a method for buffer management in a disk drive having a first segment for storing burst data and a a second segment used for write and read commands (abstract).

6. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 746-7239

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li
Art Unit 2186

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100